AMENDMENTS TO THE SPECIFICATION

Please delete the paragraph beginning at Page 5, Line 24 to Line 26 as follows:

~~Figure 4B is a plot of aerial image intensity vs the area exposed at the resist surface and a cross sectional view of the corresponding resist profile after development according to an embodiment of the current invention.~~

Please replace the paragraph beginning at Page 13, Line 8 with the following rewritten paragraph (showing changes):

Figure 4A shows an aerial image intensity plot for light transmitted thru the reticle thru axis 4A shown in figure 2. Also shown is the resist profile after exposure and development. Intensity simulation using ~~248nm~~ 248 nm wavelength, Numerical Aperture (Na) ~~Na~~ of 0 f and partial coherency factor (σ) (sigma) of 0.5 was used to form the desired intensity profile. The use of the phase shifting layer 46 with the 180 degree shift produced small via holes. The area surrounding the hole will have low intensity, but as the area is relative small, the resist process of baking will eliminate the feature. The topographical resist profile shows a via hole and trench line in which metal can be formed (in the subsequently patterned dielectric layer) .

Please delete the Heading and paragraphs beginning on page 13, line 16 to line 20, as follows:

~~*A. Figure 4B*~~

~~Figure 4B shows a plot of aerial image intensity vs the area exposed at the resist surface.~~

~~The semiconductor structure 12 is shown with lower resist layer 20 and upper resist layer 24 after the resist layers are exposed and developed.~~